IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
PP 25-27

On The Computation of LFSR Characteristic Polynomials for Built-In Deterministic Test Pattern Generation

Mrs M.NANDHINI, M.E –VLSI Design Mr. J. SUDHAKAR., M.E., (Ph.D)
SUPERVISOR & Asst Prof.
Department of Electronic and Communication Engineering , Thirumalai Engineering College
Kilambi, Kancheepuram-631551

Abstract: *In the production of integrated circuits, testing is done to identify defective chips.An efficient LFSR polynomial computation to generate all possible test from test set & to achieve 100% fault coverage. To compute more efficient seed sets for highest randomization. Randomization of LFSR through seed changes and polynomial changes. The efficiency of randomized LFSR in transition reduction Leads to power reduction.*
In VLSI testing equipments generated input patterns are applied to CUT through scan cells in a serial manner (shift and scan method). The scan chain length is increased linearly with number of flip flops in CUT. In multiple scan chain scan cells will be grouped and test patterns will be applied to CUT in a parallel. In this scan design testing; all selected storage elements are replaced by scan cells.

I. Introduction

The main objective is to carry out efficient LFSR polynomial computation to generate all possible test from test set & to achieve 100% fault coverage. To compute more efficient seed sets for highest randomization. The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. Hence the important aspect to optimize power during testing. Power dissipation is a challenging problem for today's System-on-Chips (SoCs) design and test. Automatic test equipment (ATE) is the instrumentation used in external testing to apply test patterns to the CUT, to analyze the responses from the CUT, and to mark the CUT as good or bad according to the analyzed responses. ATE has a serious disadvantage, since the ATE (control unit and memory) is extremely expensive and cost is expected to grow in the future as the number of chip pins increases. Built-In Self-Test (BIST) is a Design-for-Testability (DFT) technique. It eliminates the need for expensive testers. It provides fast location of failed units in a system because the chips can test themselves concurrently.

II. Existing System

In Pseudorandom Built-In Self Test (BIST) generators have long been successfully utilized for the testing of integrated circuits and systems. The arsenal of pseudorandom generators includes Linear Feedback Shift Registers (LFSRs) [1], Cellular Automata [2] and Accumulators accumulating a constant value [3]. Here LFSR pattern out is applied independently to all the target faults and optimal seeds selection is carry out. To carry out non test cubes driven seed computation for hard-to-detect faults.

Therefore, multiple weight assignments have been suggested in cases where different faults require biases of the input combinations applied to the circuit, to ensure that a relatively small number of patterns detect all faults.

III. Proposed System

In The standard LFSR method has been used as the test pattern generator for the BIST. An LFSR is a shift register where the input is a linear function of two or more bits (taps). It consists of D flip-flops and linear exclusive-OR (XOR) gates. It is considered an external exclusive-OR PRNG as the feedback network of the XOR gates feeds externally from X0 to Xn-1. Randomization can be triggers by changing both the two main parts of an LFSR such as seed values and polynomial structure of it. A shift register is used to shift its contents into adjacent positions within the register or, in the case of the position on the end, output of the register.

There are different classifications of test patterns are available in testing they are.,
· Deterministic Test Patterns
· Algorithmic Test Patterns
· Exhaustive Test Patterns

· Pseudo-Exhaustive Test Patterns
· Random Test Patterns
· Pseudo-Random Test Patterns

A BIST application may make use of a combination of different test patterns say pseudo-random test patterns may be used in conjunction with deterministic test patterns so as to gain higher fault coverage during the testing process.

PROPOSED METHODOLOGY:

A more realistic objective is to achieve the same coverage as the given deterministic test set, not necessarily using the same tests. The test generation always starts with a set of pure random patterns, to detect easy to- detect faults at low hardware cost.

The aim is to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Several low-power approaches have also been proposed for scan-based BIST. It will modify scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains with many scan enable (SE) inputs to activate one scan chain at a time, the TPG proposed in [18] can reduce average power consumption during scan-based tests and the peak power in the CUT. The data compressions considered in this field have the disadvantage of some loss of information.

IV. Architecture Diagram

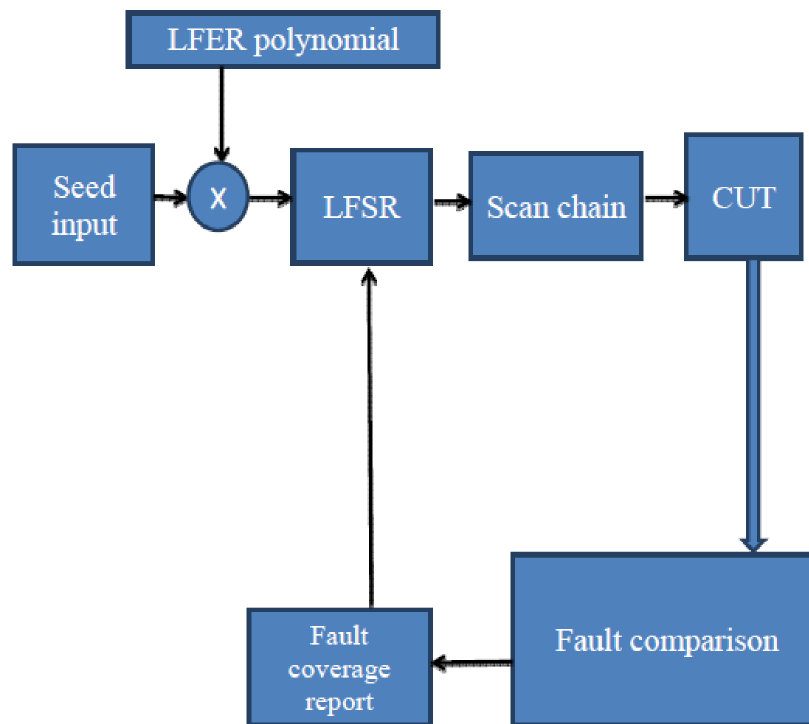

Figure.3.2: Block Diagram Propsed System.

V. Conclusion

In this thesis work by reducing the number of clock cycles and the number of ATE channels in compression methods with minimal hardware complexity. The efficiency of proposed decompression method proved that it eliminates the LFSR lockout. The proposed skipping LFSR provides similar channel separation as the LFSR with a phase shifter but the hardware overhead is lower than the originally introduced solution of the Smart BIST. The number of LFSR flip-flop XORed in parallel with the test volume and the number of parallel scan chains loaded from the decompressor on the length of test sequence. In order to reduce the testing time the Scan cells are connected into multiple shift registers and more number of clock cycles are needed to access the particular register is depends on register position from boundaries.Become inefficient to test deep registers and due to continuous switching from all register testing time will be very high. In future work we propose single cycle access structure: Test patterns can be applied to any part of CUT with single clock cycle period.

Future work

To extend the research topic of fault coverage reconfigurable multiple polynomials can be used in LFSR generation phase. Parallel Signature Analyzer (PSA) can also be used for high speed testing. In order to support wide range of scan chain length and to avoid fault masking multiple scan chain with dynamic shifting will be useful.

References

[1]. Abu-Issa A and Quigley S. "Bit-swapping LFSR and scan-chainordering: A novel technique for peak- and average-power reduction inscan-based BIST," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., 2009 vol. 28, no. 5, pp. 755–759.

[2]. Bhunia S, Mahmoodi H, Ghosh D, Mukhopadhyay S and Roy K."Lowpower scan design using first-level supply gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2005, vol. 13, pp. 384–395

[3]. Bonhomme Y, Girard P, Guiller L, Landrault C and Pravossoudovitch S. "A gated clock scheme for low power scan testing of logic ICs or embedded cores," in Proc. 10th Asian Test Symp., 2001, pp.253–258.

[4]. Corno F, Rebaudengo M, Reorda M & Violante M. "A new BIST architecture for low power circuits," in Proc. Eur. Test Workshop, 1999, pp. 160–164.